	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 6242306 B1	20010605	9	Dual bit isolation scheme for flash memory devices having polysilicon floating gates	438/262	438/257	Pham, Tuan et al.
2	US 5414693 A	19950509	11	Self-aligned dual-bit split gate (DSG) flash EEPROM cell	365/185.1	257/315; 257/316	Ma, Yueh Y. et al.
3	US 5021999 A	19910604	15	Non-volatile semiconductor memory device with facility of storing tri-level data	365/185.03	257/316; 365/104; 365/185.1; 365/185.11; 365/185.16; 365/185.32; 365/189.01; 365/230.06	Kohda, Kenji et al.
4	US 6366500 B1	20020402	22	Process for making and programming and operating a dual-bit multi-level ballistic flash memory	365/185.29	365/185.14	Ogura, Seiki et al.
5	US 6248633 B1	20010619	23	Process for making and programming and operating a dual-bit multi-level ballistic MONOS memory	438/267	438/287	Ogura, Seiki et al.
6	US 6133098 A	20001017	23	Process for making and programming and operating a dual-bit multi-level ballistic flash memory	438/267		Ogura, Seiki et al.